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**Supporting Information**

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**Batch fabrication of high performance planar patch-clamp devices in quartz**

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***Ni film anodic etching***

Ni was evaporated at various thicknesses onto polished wafer substrates at a rate of 1 Å/s with a Mark 40 Electron-Beam Evaporator (CHA Industries, Fremont, CA). The substrates were either polished Si wafers (Virginia Semiconductor, Fredericksburg, Virginia), polished Si wafers with low temperature oxide (LTO) deposited onto them, or fused quartz wafers (Structure Probe, Inc., West Chester, PA). For the 500 and 600 nm thick Ni films, a 20nm thick titanium film was first evaporated (1Å/s) onto the substrate as an adhesion layer. Either electron-beam or photolithography was used to pattern features into 950 PMMA (MicroChem Corp, Newton, MA) or AZ5214E (AZ Electronics, Branchburg, NJ) resist films, respectively. The PMMA and AZ5214E resist was diluted with chlorobenzene (Sigma Aldrich, St. Louis, MO) and Propylene Glycol Methyl Ether Acetate (Sigma Aldrich), respectively, in order to obtain the appropriate resist thickness. The Ni surface was contacted with an 'alligator' clip on the top of the wafer, while the rest of the wafer was submerged into Class 10 85% (wt) phosphoric acid (General Chemical, Parsippany, New Jersey). Biases were applied to the substrates with an E3611A DC Power Supply (Agilent Technologies, Inc, Santa Clara, CA). After the anodic etching, the resist was removed by dissolving in Class 10 acetone (General Chemical). See Table S.1 for exact processing parameters.

***Plasma etching of $SiO_2$***

The pores in the 0.5 μm thick $SiO_2$ membrane that were used as planar patch-clamp electrodes (Figure 4A) were patterned into a Cr masking layer with standard lithography techniques and transferred into a thermally-grown $SiO_2$ layer with a Unaxis SLR 720 Reactive Ion Etcher (OC Oerlikon Corporation, Switzerland) with the electrode operated at 40MHz. LTO films and fused quartz wafers (Structure Probe, Inc) were utilized for 2.5-5 μm thick and 7.6-12 μm thick $SiO_2$, respectively. LTO films were deposited on Si wafers with resistivities >1 Ωcm (Virginia Semiconductor) in a low pressure chemical vapor deposition (LPCVD) tube furnace (Tystar Corporation, Torrance, CA). To reduce film stress in the 5μm thick LTO

films, we deposited approximately 2.5 μm of LTO, annealed the wafer at 1000°C for 1 hour, and then deposited approximately an additional 2.5 μm thick LTO film. The thickness of the $SiO_2$ films on Si substrates was directly measured with a Nanospec 210 (Nanometrics Incorporated, Milpitas, CA) interferometer. Patterns in the nickel masking film were transferred into the $SiO_2$ with an Advanced Oxide Etcher (Surface Technology Systems, PLC, Newport, UK). Before etching HAR structures, we cleaned the etching chamber with an $O_2$ plasma, and then 'seasoned' the chamber with the etching recipe on a blank Si wafer for 20 minutes*[1]*. See Table S.2 for exact plasma processing parameters. For the wafers utilized as planar patch-clamp electrodes, underside trenches (Figure 1B) were etched with either a Unaxis SLR 770 Deep Reactive Ion Etcher (OC Oerlikon Corporation) while masked with a photoresist film (for the 0.5 μm thick $SiO_2$ devices), EDP Type F etchant *[2]* while masked with a $SiO_2$ film with the front side protected by an evaporated gold film and a PEEK wafer holder (for 1.5-5.0 μm thick LTO devices), or Class 10 49% HF(aq) (General Chemical) etchant while masked with a 600 nm thick evaporated gold film with the front side protected by a Teflon wafer holder (for fused quartz devices). The thickness of the reulting suspended membranes in the fused quartz substrates was directly measured with a Wyko NT3300 (Veeco Metrology Inc., Tucson, AZ) interferometer.

***Monte Carlo Simulations of HAR Dielectric Etching***

A specific dielectric pore geometry is assumed (Figure S4 A) while the mask thickness is varied, thus, altering the aspect ratio. First, a bi-modal ion energy distribution function is calculated from the Lieberman model*[3]* (Figure S4 B) with the following assumptions: The plasma density is $10^{13}/cm^3$. The ion temperature is 0.5eV and the mean electron temperature is 6eV, determined from a Maxwell distribution with an isotropic angular distribution. The sheath voltage is $V_{sh} = 0.5V_{rf}(1 + \sin \omega_{rf}t) + V_{DC}$, where $V_{rf} = 50V$, $\omega_{rf} = 10MHz$, and $V_{DC} = 10.5V$. After particle generation, by randomly sampling the corresponding distributions, particles were tracked using the following equations of motion:

$$m\frac{d\mathbf{v}}{dt} = q\mathbf{E} \qquad \frac{d\mathbf{x}}{dt} = \mathbf{v}$$

$$\mathbf{E} = (1-\bar{x})(1-\bar{z})\mathbf{E}_{0,0} + (\bar{x})(1-\bar{z})\mathbf{E}_{1,0} + (1-\bar{x})(\bar{z})\mathbf{E}_{0,1} + (\bar{x})(\bar{z})\mathbf{E}_{1,1}$$

The fourth order Runge Kutta method is used to solve the derivatives. Electric fields were calculated using finite differences on certain particle positions. In the gas phase, the charge density is low, so Laplace's equation can be solved iteratively to update the potentials as more charge accumulates:

$$\nabla^2 \phi = 0$$

In the case of surface collisions, the conjugate gradient method was used to update the potentials. The potentials on the metal were treated as zero, while the potentials on dielectric surfaces were calculated using Gauss's law, which is the function of the surface charge density.

$$\mathbf{n} \cdot \nabla \phi = -\frac{\sigma}{\varepsilon_0}$$

Steady state is reached when the potential distributions on the insulator walls no longer change.

***Cell Culture and harvesting***

All cell lines and reagents were purchases from the American Type Culture Collection (ATCC, Manassas, VA). CHO-K1 (#CRL-9618) and RBL-1 (#CRL-1378) cells were used investigate the cell patching clamping capabilities of the planar patch-clamp devices. The cell lines were maintained at 37$^o$C in a 5% $CO_2$ atmosphere. The ATCC suggested media was supplemented with 10% (v/v) fetal bovine serum (FBS), 1% (v/v) penicillin (100 mg/ml), 1% (v/v) streptomycin (100 mg/ml). Cells were grown and passaged according to the ATCC guidelines. When the adherent CHO cells were confluent, the cells were detached from the culture flask by exposing it to trypsin for 1-2 min. Optimal electrophysiology results (seal yield) for the suspended RBL cell line was obtained when cells were cultured for roughly 18-24 hours and harvested at $\geq$5 x $10^5$ cells/mL. To harvest the cells for electrophysiology measurements, cells were spun down at 500-800 RPM and then washed with saline solution three times.

***Electrophysiology Recordings with planar electrodes***

The wafer packaging scheme has been previously described *[4]*. A Multiclamp 700A was driven by the Multiclamp Commander software and interfaced with pClamp 8 acquisition software using a Digidata 1322A. The recorded data was analyzed with Clampfit 8 software. The amplifier, digitizer, and software were all purchased from MDS Analytical Technologies (Sunnyvale, CA). When testing seals, the intracellular solution (bottom-side) contained (in mM) 130 KCl, 5 NaCl, 2.5 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, pH=7.4 with a final osmolarity of 265 mOs. The extracellular solution (top-side) contained (in mM) 130 NaCl, 5 KCl, 10 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, pH=7.4 (adjusted with NaOH) with a final osmolarity of 293 mOs. For some of the trials with 1.5-2.6μm and 3.0μm deep pores, the majority of the chloride ions

were replaced with either glutamate or aspartate to investigate the influence of ions in achieving gigaohm seals. We observed no difference in sealing performance.

To introduce cells into the planar patch-clamp platform, approximately 10μL of a cell suspension (roughly $5x10^5$ cells in 1 mL of recording solution) was pipetted into the top recording chamber (Fig. 2b). Suction (5-30 mbar) was applied from the bottom chamber to immobilize cells over the pore. Then negative pressure in the range of 5-150 mbar was gradually applied while monitoring the resistance across the pore. The holding potential was gradually decreased to -60 mV to help induce seal formation in some cases. Once the seal reached 1 GΩ or higher, the suction was released. For the whole cell measurement in Fig. 4c, the intracellular solution contained (in mM) 130 KCl, 5 NaCl, 4 $CaCl_2$, 2.1 $MgCl_2$, 10 HEPES, 10 EGTA with pH=7.4. The extracellular solution contained (in mM) 130 KCl, 5 NaCl, 10 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, pH=7.4. Current traces were acquired at 20 kHz and filtered at 1 kHz. Capacity transients were manually removed to focus on the ion channel currents.

CHO cells were used to test seals for the 0.5-2.6 μm deep pores. CHO and RBL cells were both used to test seals for the 3.0 μm deep pores. RBL cells were used to test seals for 5.0-12 μm deep pores (see Table S3). The deepest pores that produced 0% GΩ seals (3 μm deep) pores were with both CHO and RBL cells. All deeper pores were investigated with just RBL cells. Thus, a single cell type was investigated as the pore depth was increased from 3 μm (0% GΩ seals) to >7 μm (78% GΩ seals), which is most important part of the Fig 4B curve. Further, it has been previously demonstrated that CHO and RBL cells have similar GΩ seal yields for a single device design*[5]*; hence, the trend of GΩ seal yield vs pore depth (Fig. 4b) represents the real influence of pore depth, and not an influence of cell type.

The 0.5 μm and 1.5-5.0 μm deep pores were fabricated in thermally-grown $SiO_2$ and annealed, LTO films on silicon, respectively, while the 7.6-12 μm deep pores were fabricated in fused quartz (see Table S3). A single material (LTO) was investigated through the inflection point in Fig. 4b (3.0 μm → 5.0 μm), demonstrating the smoothness and depth of the pore is most important for seal yield, not the nature of the $SiO_2$. We note that traditional patch-clamp experiments are successfully done with a host of different $SiO_2$ pipette compositions*[6]*, and so part of our motivation of investigating the different compositions here was to demonstrate that the nature of the $SiO_2$ is not important for seal yield - it is the smoothness and the depth of the pore.

***References***

[1] M. Schaepkens, R. C. M. Bosch, T. Standaert, G. S. Oehrlein, J. M. Cook, *J. Vac. Sci. Technol. A-Vac. Surf. Films* **1998**, *16*, 2099.
[2] A. Reisman, M. Berkenblit, S. Chan, F. Kaufman, D. Green, *J. Electrochem. Soc.* **1979**, *126*, 1406.
[3] M. Lieberman, A. Lichtenberg, *Principles of plasma discharges and materials processing*, Wiley-Interscience, **2005**.
[4] R. Pantoja, J. Nagarah, D. Starace, N. Melosh, R. Blunck, F. Bezanilla, J. Heath, *Biosensors and Bioelectronics* **2004**, *20*, 509.
[5] K. Klemic, J. Klemic, F. Sigworth, *Pflügers Archiv European Journal of Physiology* **2005**, *449*, 564.
[6] D. P. Corey, C. F. Stevens, in Single Channel Recording, (Eds: B. Sakmann, E. Neher), Plenum Press, New York **1983**, Ch. 3.

**Table S.1. Anodic etching parameters for Ni films**

| Figure | Ni film thick-ness | Resist-defined Diameter | Resist thickness | 1st applied bias | Time (sec) | 2nd applied bias | Time (sec) | Ni diameter |
|---|---|---|---|---|---|---|---|---|
| **2A** | 250nm | 100nm | 230-270nm | 2.0V | 50 | 2.2V | 160 | 1.4μm |
| **2B #1** | 100nm | 70nm | 230-270nm | 2.2V | 45 | - | - | 300nm |
| **2B #2** | 300nm | 100nm | 230-270nm | 2.0V | 50 | 2.2V | 120 | 1.5μm |
| **2B #3** | 500nm | 300nm | 230-270nm | 3.4V | 600 | - | - | 1.4μm |

**Table S.2. Plasma parameters for high-density plasma etching $SiO_2$ films**

| Fig. | $SiO_2$ thick-ness (μm) | Ni mask thick-ness (nm) | ICP Power (watts) | RIE Power (watts) | $C_4F_8$ (sccm) | $CF_4$ (sccm) | $O_2$ (sccm) | He (sccm) | p (mT) | Etch time (min) |
|---|---|---|---|---|---|---|---|---|---|---|
| **2D#1** | 3 | 150 | 1000 | 300 | 26 | - | - | 50 | 8 | 6.0 |
| **2D#2** | 5 | 300 | 1000 | 300 | 40 | - | 5 | - | 6 | 9.5 |
| **2D#3** | 8 | 400 | 1000 | 250 | 40 | - | 1 | - | 6 | 15 |
| **3A** | 5 | 250 | 1000 | 300 | 40 | - | 5 | - | 6 | 9 |
| **3A** | 5 | 275 | 1000 | 300 | 40 | - | 5 | - | 6 | 9 |
| **3A** | 5 | 400 | 1000 | 300 | 40 | - | 5 | - | 6 | 9 |
| **3A** | 5 | 600 | 1000 | 300 | 40 | - | 5 | - | 6 | 10 |
| **4A (not shown)** | 1.5-2.6 | 150 | 1400 | 55 | - | 20 | - | 220 | 4 | 14 |
| **4A (not) shown)** | 3.0 | 150 | 1000 | 300 | 26 | - | - | 50 | 8 | 6 |
| **4A (not) shown)** | 5.0 | 275 | 1000 | 300 | 40 | - | 5 | - | 6 | 8 |
| **4A (not) shown)** | 7.6-12 | 400 | 1000 | 250 | 40 | - | 1 | - | 6 | 15-23 |

**Table S.3. Cell and $SiO_2$ type used for planar patch-clamp experiments**

| **Material:** | *Thermal $SiO_2$* | *LTO* | *LTO* | *LTO* | *quartz* |
|---|---|---|---|---|---|
| **Pore depth (μm)** | 0.5 | 1.5-2.6 | 3.0 | 5.0 | >7.0 |
| **# trials** | 6 | 33 | 37 | 17 | 18 |
| **# GΩ seals** | 0 | 0 | 0 | 7 | 14 |
| **% GΩ seals, CHO cells** | 0% | 0% | 0% | - | - |
| **% GΩ seals, RBL cells** | - | - | 0% | 41% | 78% |

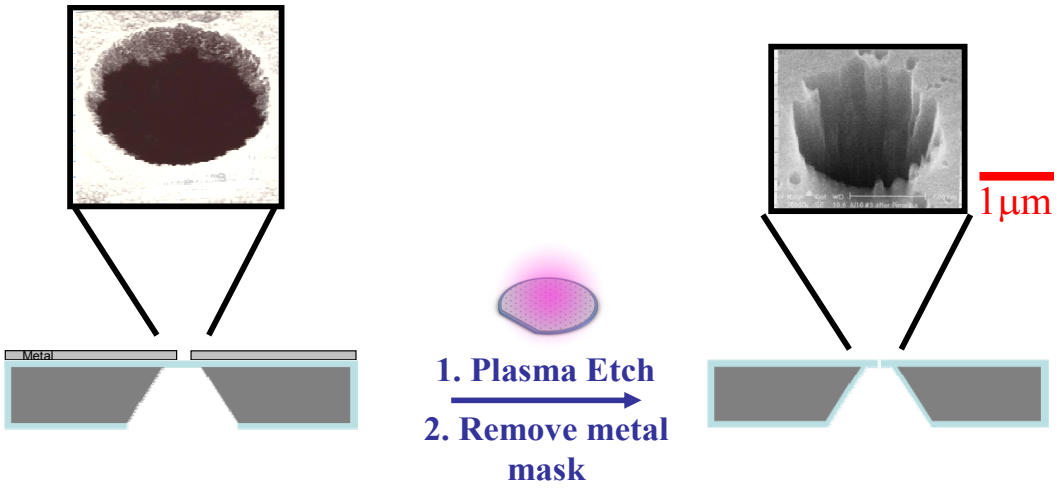


**Figure S1. High-density plasma etching with a poorly prepared mask. A.** SEM image of a poorly prepared Ni mask. **B.** SEM image of the silicon dioxide via with very rough features after high-density fluorocarbon etching. This demonstrates smoother mask features are required to produce smooth features in dielectrics at the micron scale. The plasma etching parameters were ICP P=700W, RIE P=200W, $CHF_3$=33sccm, $C_4F_8$=7, Ar=10sccm, p=10mT, etch time=4 min.

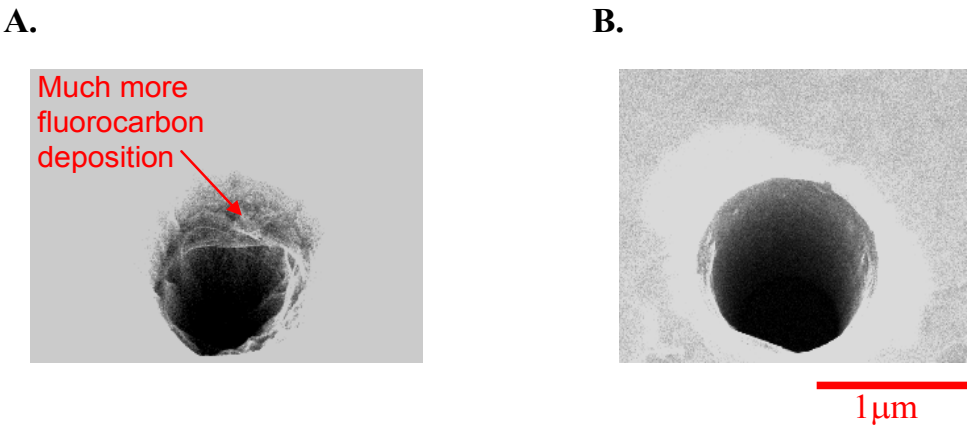


**Figure S2. Reproducibility of high-density $C_4F_8$ plasma etching of HAR structures dependence on ICP Power. A.** After a 20 min chamber 'seasoning' with an ICP P = 1400W, we noticed that the temperature meter, attached to the outside of the thick chamber walls can rise greater than 134°C (the chamber heater's thermo-couple set point is 130°C). It has been observed that the loss of fluorocarbon species to the chamber walls is reduced as the wall temperature is increased, resulting in more polymer deposition onto the wafer (Schaepkens et al., 1998). This makes sense with our data, as we show more fluorocarbon deposition on the wafer with hotter chamber walls. **B.** After a chamber 'seasoning', we waited 20 min before plasma etching $SiO_2$ to allow the chamber walls to cool. The amount of fluorocarbon polymer deposited onto the wafer is reduced. Thus, to reproducibly fabricate smooth, HAR structures in oxide, the ICP P must be low enough to maintain a constant chamber wall temperature. The plasma etch parameters for the chamber 'seasoning' and $SiO_2$ etching above were ICP P = 1400W, RIE P = 150 W, $C_4F_8$ = 40sccm, $O_2$ = 5sccm, pressure = 6mT, etch time = 5 min. The Ni mask and $SiO_2$ film were 150nm and 3.4μm thick, respectively. The pores imaged above were not cleaned after etching.

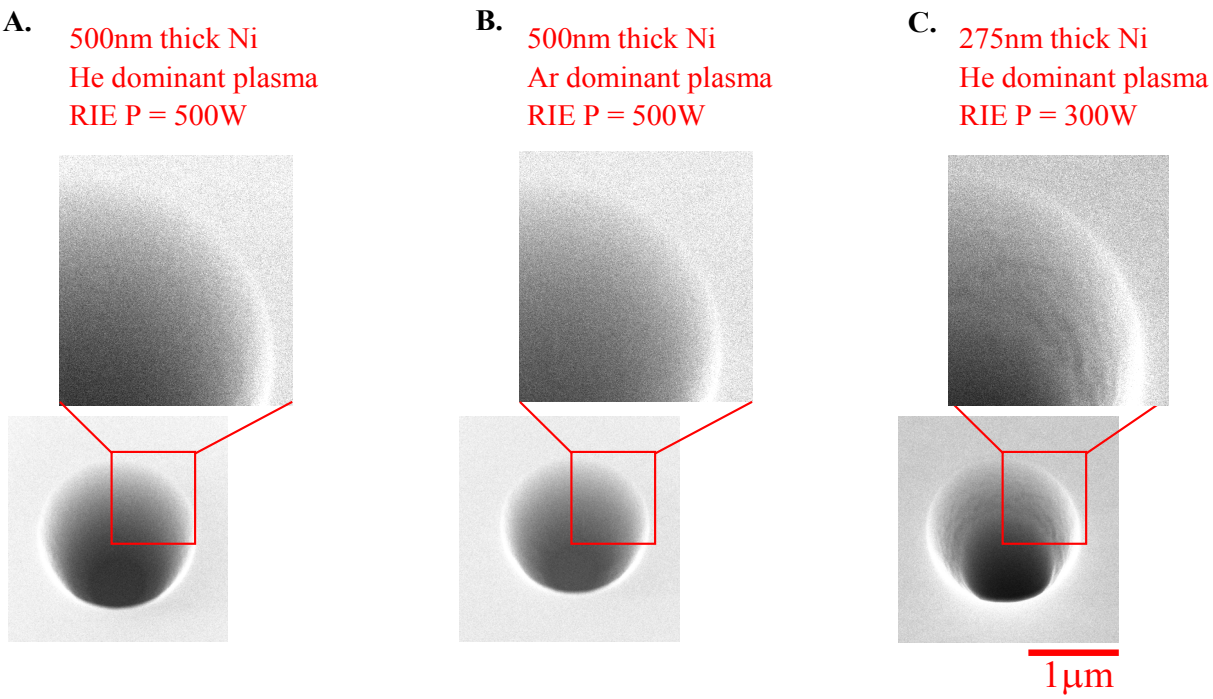


**Figure S3. $SiO_2$ pore smoothness dependence on plasma parameters.** **A.** $SiO_2$ pore etched with a 500nm thick Ni mask with the following parameters: RIE P=500W, He=50sccm, time= 8min. **B.** $SiO_2$ pore etched with a 500nm thick Ni mask with the following parameters: RIE P=500W, Ar=50sccm, time= 8min. When protected by a 500nm thick Ni mask (3SA & B), the $SiO_2$ sidewalls are smooth even though they are etched with different plasma recipes than the pores in Figure 3A and with the RIE P=500W. **C.** $SiO_2$ pore etched with a 275nm thick Ni mask with the following parameters: RIE P=300W, He=50sccm, time= 10min. The $SiO_2$ pore was protected a 275nm thick Ni mask, and shows roughness similar to the hole masked with 275nm thick Ni in Figure 3A which was etched with a different plasma chemistry. For all above trials, ICP P=1000W, $C_4F_8$=26sccm, p=8mT. These results show that the trend of oxide sidewall smoothness vs. Ni mask thickness (Figure 3A) is not result of the specific plasma chemistry, validating the consideration of solely charging phenomena in the Monte Carlo simulations.

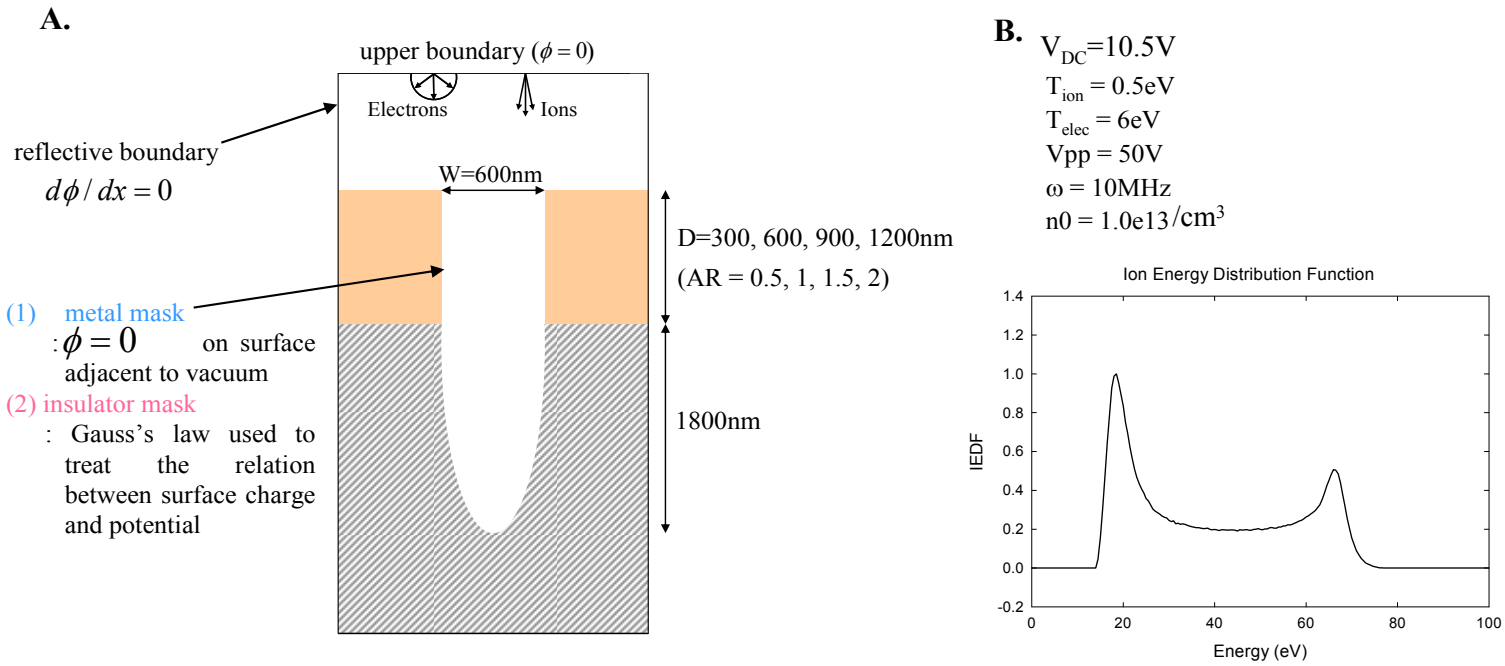


**Figure S4. Simulation Domain for Monte Carlo Simulations of high density plasma etching. A.** The simulation domain is shown. Mask thicknesses were varied to investigate charging effects from altering the aspect ratio of the pore. **B.** The specific parameters used in the simulation are shown. We used a bimodal ion energy density function (IEDF) in the simulation which was calculated from the Lieberman model.

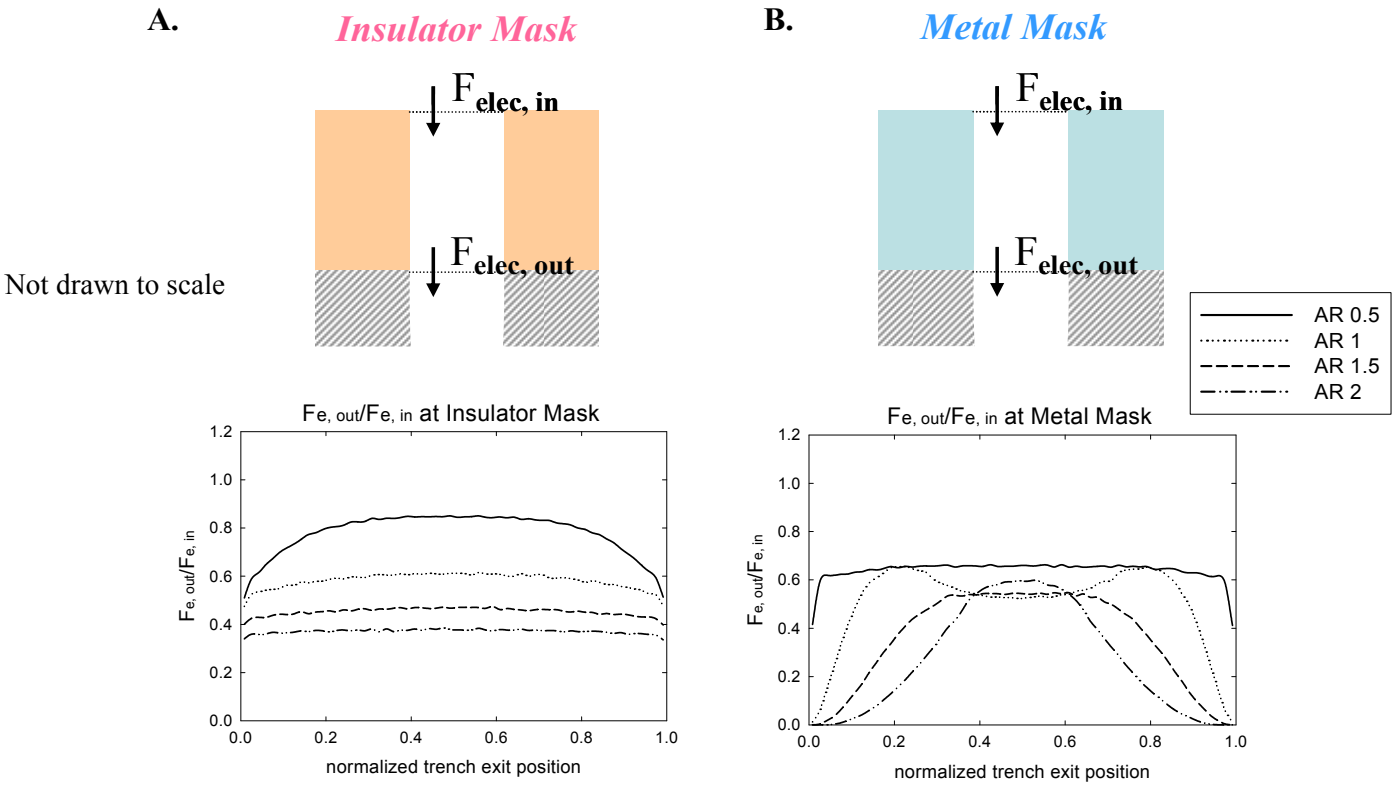


**Figure S5. Electron flux through insulating and conducting mask regions. A.** Electron flux through an insulating mask at different mask thicknesses. The smooth decrease of electron flux as the mask thickness increases is expected due to the electrons' isotropic velocity distribution. **B.** Electron flux through a conducting mask at different mask thicknesses. The electron flux shows abrupt behavior as the metal mask thickness is increased; the flux decreases significantly near the sidewalls. This is a consequence of the potential of the conducting mask surface being zero. See text for a further explanation.

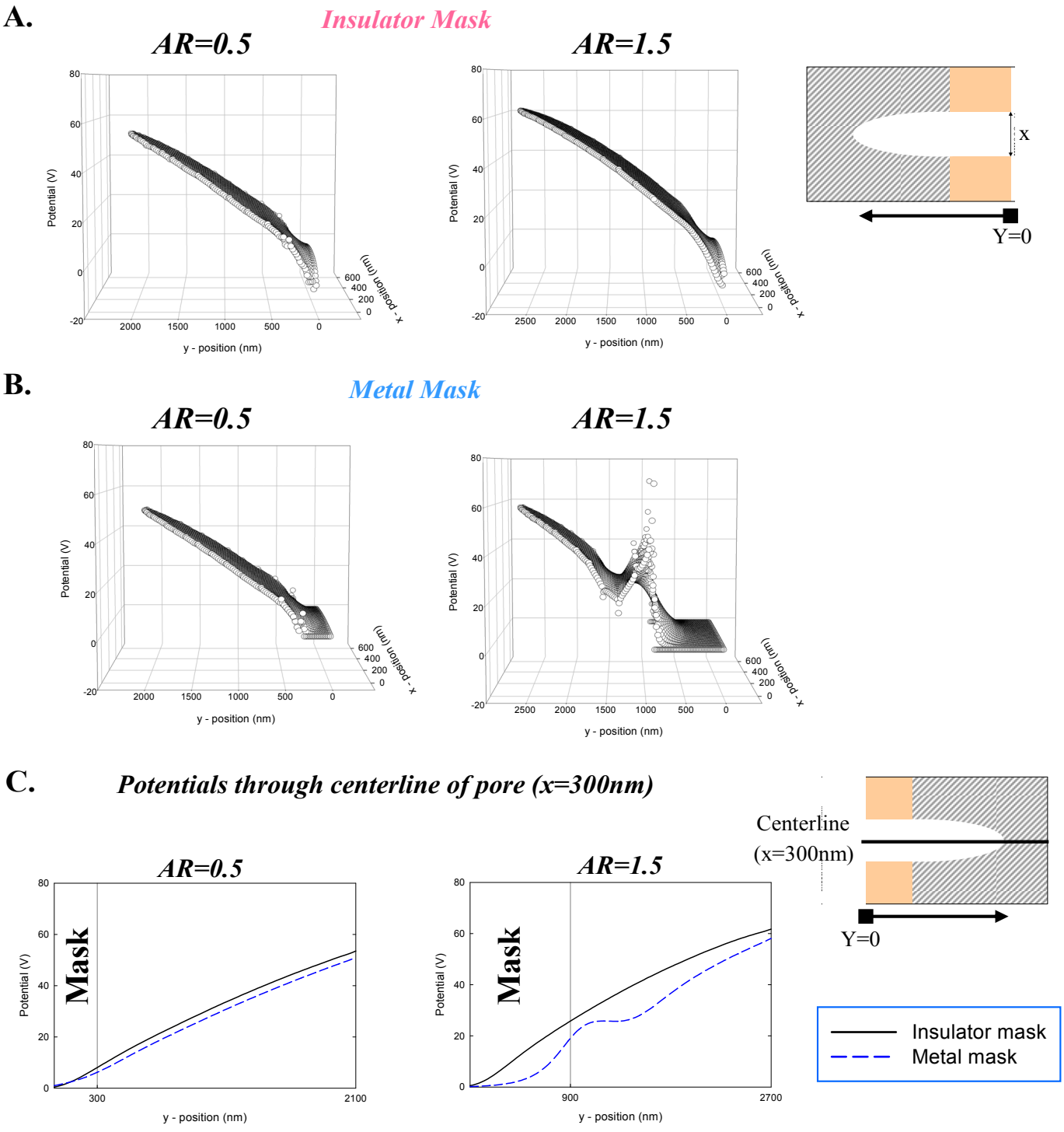


**Figure S6. Simulations of electric potential throughout HAR dielectric pores during high density plasma etching. A. & B.** The potential throughout the dielectric pore is shown for insulating and conducting mask cases at different aspect ratios. The potential within the trench must rise as a function of depth in order to balance the reduced electron current to the bottom of the trench at steady state. This behavior is similar for both the insulating and conducting mask case at AR=0.5. However, the conducting mask case at AR=1.5 shows abrupt behavior at the $SiO_2$ pore entrance when compared to the insulating mask case. See Figure S5 and text for a further explanation. **C.** While the potential near the sidewalls at the top of the pore varies drastically for the insulating and conducting mask case at AR=1.5, the potentials down the centerline of the pore are more similar. This phenomenon results in an appreciable $SiO_2$ etch rate for the conducting mask case even though there are huge retarding electric fields near the dielectric pore opening (see Figure 3C). The schematics on the right show what direction the axes correspond to in parts A-C.